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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,767	02/19/2002	Jens Graf	10191/2246	7845
26646	7590	09/15/2005	EXAMINER	
KENYON & KENYON ONE BROADWAY NEW YORK, NY 10004			NGUYEN, THAN VINH	
			ART UNIT	PAPER NUMBER

2187

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/079,767

Applicant(s)

GRAF ET AL.

Examiner

Than Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This is a response to the response, filed 7/1/05.
2. Claims 1-8 are pending.

Response to Arguments

3. Applicant's arguments filed 7/1/05 have been fully considered but they are not persuasive. Applicant argues that Norman does not teach the commands are not written to the buffers independently of one another. The Examiner disagrees. The Examiner interprets this claim "independent" language to mean that command is stored in the first buffer does not require data to be stored in the second buffer. Norman does not require that the command buffer 48 and data buffer 52 store data at the same time. Norman teaches the input buffer 48 is controlled by IEN signal and the buffer 52 is controlled by IEN signal and I/O signal (Fig. 4). It is clear that buffer 48 and 52 can be written independent of one another since the control signals are different.

4. With regards to Applicant 's arguments that motivation is not provided for the 35 USC 103 rejection, the Examiner disagrees. Applicant claims to integrate the buffers into one memory. Integration of multiple elements onto a single device/chip is well known in the art to save space and expense, with lower delays. This is further supported by In re Larson, a well known case regarding integration of multiple elements onto a single element. The Examiner maintains the rejections to the claims.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

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the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Norman et al (US 6567335).

As to claim 1:

7. Norman discloses a memory system having a memory controller connected to multiple memory devices. Norman discloses the claimed memory arrangement comprising: a programmable memory (flash memory 38; 4/48-67); a first buffer memory associated with the programmable memory, to which first buffer memory, in the case of a command access, at least one command following the accessed command is written (command buffer 48 stores/buffers commands going to command decode logic; Fig. 4; 3/5-12, 5/60-67; claim 29,32); and a second buffer memory to which, in the case of a data access, at least one datum following the accessed datum is written (data buffer 52 stores data from memory array; Fig. 4; 6/7-12, 13-20, 25-30; claim 29,32). The commands going into buffer 48 and data entering buffer 52 are written independently of one another (data going to buffer 48 and 52 are independent of one another; Fig. 4; 5/56-6/20).

Norman does not specifically teach the first buffer and second buffer is integrated in the flash memory. The courts also have found that forming a single integral element from multiple elements would be a matter of obvious engineering choice and would be obvious one of ordinary skills in the art to save space and expense, with lower delays (In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965)). Thus, it would have been obvious to one of ordinary skills in the art at the time of the invention to integrate the first and second buffers in the flash memory of Norman to save space and expense.

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As to claim 2:

1. Norman discloses the programmable memory includes a burst flash memory (flash memory 38; 4/48-67).

As to claim 3,7,8:

2. Norman teaches the second buffer memory is loaded only in the case of a data access (data input buffer 52 stores temporary data upon read; 6/7-12, 13-20,25-30; 8/40-50).

As to claim 4:

3. Norman teaches content of the first buffer memory (command input buffer 48-51) is not changed when the at least one datum is subsequently read from the second buffer memory (command buffer 48 and data buffer 52 not affected by one another (Figure 4).

As to claims 5-6:

4. Norman discloses a memory system having a memory controller connected to multiple memory devices. Norman discloses the claimed method for performing at least one of a command access and a data access during a program execution in connection with a programmable memory, comprising the steps of: recognizing in the case of a command access that a command access is present; recognizing in the case of a data access that a data access is present; writing a command following the accessed command to a first buffer memory; and writing a datum following the accessed datum to a second buffer memory (command input buffer 48 stores/buffers commands going to command decode logic; Fig. 4; 3/5-12, 5/60-67; claim 29,32; data buffer 52 stores data from memory array; Fig. 4; 6/7-12, 13-20, 25-30; claim 29). The commands going into

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buffer 48 and data entering buffer 52 are written independently of one another (data going to buffer 48 and 52 are independent of one another; Fig. 4; 5/56-6/20). Norman does not specifically teach the first buffer and second buffer is integrated in the flash memory. It is well known in the art of memory design to integrate multiple devices onto a single chip to provide for faster access, smaller footprint/size, and reduced cost. The courts also have found that forming a single integral element from multiple elements would be a matter of obvious engineering choice and would be obvious one of ordinary skills in the art (*In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965). Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to integrate the first and second buffers in the flash memory of Norman.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571)272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Than Nguyen
Examiner
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